Lab 5 – Digital I/O

Digital electronics is the heart and soul of modern computers. The ability to set and read digital lines is essential to digital circuit diagnostics.



Figure 5.0. Four bit Digital Counter Circuit on NI ELVIS II Protoboard

Goal: This lab focuses on NI ELVIS II digital tools, such as a digital clock, digital counter, and a logic state analyzer, to study digital circuits.

Required Soft Front Panels (SFPs)

Digital writer (DigOut) Digital reader (DigIn) FGEN (TTL outputs) Oscilloscope (Scope)

Required Components

 $\begin{array}{l} 10 \ k\Omega \ resistor \ R_A \ (brown, \ black, \ orange) \\ 100 \ k\Omega \ resistor \ R_B \ (brown, \ black, \ yellow) \\ 1 \ \mu F \ capacitor \ C \\ 555 \ timer \ chip \\ 7493 \ 4\ bit \ binary \ counter \end{array}$

Exercise 5.1: Visualizing Digital Byte Patterns

The NI ELVIS II protoboard has a bank of eight green LEDs with input pin sockets labeled LED <0 .. 7>. You can use them as visual indicators of digital logic states (On = HI and Off = LO).

Complete the following steps to output a digital pattern using the Digital Writer:

1. Wire the LEDs <0..7> to the corresponding socket pins labeled DIO <0..7>. For example, connect DIO 0 alias line 0 to the pin socket LED <0>. Only one lead is required because the grounds are connected internally within NI ELVIS II.

Note: The digital I/O lines are located on the right side of the protoboard.

- 2. Launch the NI ELVIS II Instrument Launcher strip.
- 3. Select the **Digital Writer** (**DigOut**) icon.

A new digital logic diagnostic window opens, so you can set/reset any of the digital lines to a HI or LO state. By default, the digital I/O lines <0..7> are selected from the three 8-bit ports in the Lines to Write box.

🗱 NI ELVISmx Digital Writer 📃 🗖 🔀
Labylew Numeric Value × 0 Line O O O O States O O O O O 7 6 5 4 3 2 1 0
Configuration Settings Lines to Write 0 - 7
Pattern Manual
Manual Pattern * 55 Lines: 7 6 5 4 3 2 1 0
Action Direction Toggle Rotate Shift Left 💟
Instrument Control Device Generation Mode Dev3 (NI ELVIS II) C Run Stop Help C

Figure 5.1. Dig Out front panel window

The digital output lines are labeled 0 to 7 reading right to left in the Manual Pattern box. You can set/reset (HI/LO) any bit by clicking on the top or bottom portion of the virtual switch. Collectively, these 8 bits constitute a byte that can be read in a binary, octal, hexadecimal, or decimal format, or in an SI notation in the display box above the switches. By clicking on the grayed-out portion, you can set the radix (format) of this indicator.

Binary	Hexadecimal	Decima
11000011	× C3	₫ 195

Figure 5.2. LabVIEW indicators for Binary, Hexadecimal or Decimal Displays

4. After you have set a digital pattern, turn on the power to the protoboard and click **Run** (green arrow) to send the pattern to the parallel output digital I/O lines <0 ... 7>, which in turn are passed on to the green LEDs.

Note: You can set the Generation Mode to output a single pattern or to continuously output the pattern. In continuous operation, the hardware is updated continuously with the current pattern.

The set pattern is echoed on the line states (blue LED indicators) of the Bus State on the SFP. Also, with the Action buttons of the SFP, you can toggle, rotate, or shift the bit pattern right or left.

5. Press the **Stop** button (red box) to cease updating the port.

In testing a digital circuit, you can select from several commonly used patterns for diagnostic checks.

6. Click the **Pattern** selector on the SFP to view the options available.

Manual	Load any 8-bit pattern
Ramp (0 – 255)	Computer Instruction INC
Alternating 1/0s	Computer Instruction INVERT
Walking 1s	Computer Instruction SHIFT LEFT LOGIC

- 7. Try to output each bit pattern.
- 8. Close the **Digital Writer** window.

End of Exercise 5.1

Exercise 5.2: 555 Digital Clock Circuit

You can configure a 555 timer chip, together with resistors R_A , R_B , and capacitor C, to act as a digital clock source.



Figure 5.3. 555 Digital Clock Circuit

Complete the following steps to build and perform measurements on a 555 digital clock circuit:

1. Using the DMM[Ω] and DMM[C], measure the component values and complete the following table.

R _A	 Ω (nominal 10 k Ω)
R _B	 Ω (nominal 100 k Ω)
С	 μF (nominal 1 μF)

2. Build the clock circuit on the protoboard as shown below.



Figure 5.4. 555 Timer chip Configured as a Digital Oscillator

Power (+5 V) goes to pins 8 and 4, and GROUND goes to pin 1. The timing chain of R_A , R_B , and C straddles the power supply. It has a connection between the resistors going to pin 7 and a connection between R_B and C going to pins 2 and 6.

- 3. Wire the 555 output pin 3 to one of the port pin sockets, DIO <0>.
- 4. From the NI ELVIS II Instrument Launcher strip, select the **Digital Reader** (**DigIn**) icon.

By default the second 8-bit port is set to input (Lines to Read 8-15).

5. Configure Lines to Read to (0-7), enable power to the protoboard, and click **Run**.

😫 NI ELVISmx Digital Reader 🛛 🔳 🗖 🗙
Numeric Value × 1
Line States 🔿 🔿 🔿 🌍 🌍 🌍 🌍
7 6 5 4 3 2 1 0
Configuration Settings Lines to Read 0 - 7
-Instrument Control
Device Acquisition Mode
Dev3 (NI ELVIS II)
Run Stop Help

Figure 5.5. Digital Writer reading bit 0, line DIO <0>

The **Digital Reader** allows the current state of a parallel input port to be read on demand (single shot) or continuously. You should see the state of line 0 flashing. If not, click on the **Stop** button and use the DMM[V] to check voltage levels on the 555 pins (stop the **Digital Reader** first).

With the clock circuit running, you can now make some useful digital circuit measurements.

The 555 timer oscillator circuit has a Period T of

 $T = 0.695 (R_A + 2 R_B) C$ (seconds)

The 555 timer oscillator frequency is related to the period by

F = 1/T (Hz)

The 555 timer oscillator circuit has an On time of

 $T = 0.695 (R_A + R_B) C$ (seconds)

The 555 timer oscillator circuit has a Duty Cycle (On time/period) of

$$DC = (R_A + R_B) / (R_A + 2 R_B)$$

- 6. Close all SFPs and launch the Oscilloscope (Scope) icon.
- 7. Connect the front panel BNC CH 0 input leads to pin 3 of the 555 timer chip and any ground. **Click Run.** You should now be observing the digital waveform on Channel 0 of the oscilloscope.
- 8. Select Trigger Type: Edge, Source: Chan 0 Source and Level (V) to 1.0. Your signal should be a TTL signal with an amplitude of 4 V or more, and the signal should be steady.
- 9. Observe the frequency in the scope window for CH 0.
- 10. Click the box Cursors On box and note that C1 and C2 are set to CH 0.
- 11. By clicking and dragging the cursors, measure the period, the on time, and the duty cycle. Calculate the frequency from the period measurement.
- 12. Fill in the following table:

Т	=	 (seconds)
T_{on}	=	 (seconds)
DC	=	
F	=	 (Hz)

13. Compare your measurements with the previous theoretical predictions.

14. Close any SFPs.

End of Exercise 5.2

Exercise 5.3: Building a 4-Bit Digital Counter

Complete the following steps to build a 4-bit digital counter.

- 1. Insert a 7493 four-bit binary ripple counter into the protoboard next to the 555 digital clock circuit. The 7493 chip contains a divide-by-two and a divide-by-eight counter.
- 2. Configure the chip as a divide-by-16 counter by connecting a jumper wire from pin 12 (Q1) to pin 1, Clock 2 (C2), on the 7493 chip, as shown in Figure 5.6.



Figure 5.6. Schematic Diagram 4-bit Binary Counter

- 3. On the 7493 binary counter chip, connect +5 V power to pin 5 and ground to pin 10.
- 4. Ensure that 0set inputs pins 2 and 3 are grounded.
- 5. Connect the outputs Q1, Q2, Q4, and Q8 to the LED and digital input ports of the NI ELVIS II protoboard using the following mapping scheme:

Q1 pin 12	to	DIO<0> and LED<0>
Q2 pin 9	to	DIO<1> and LED<1>
Q4 pin 8	to	DIO<2> and LED<2>
Q8 pin 11	to	DIO<3> and LED<3>
555 pin 3	to	DIO<7> and LED<7>

- 6. Connect the 555 digital clock output (pin 3) to the 7493 Clock 1 (C1) input (pin 14).
- 7. Power the protoboard and watch the binary counts accumulate on the LEDs.
- 8. Launch the NI-ELVISmx **Digital Reader** (**DigIN**) icon. Monitor the binary states on the computer screen, and, at the same time, see the states on the green LEDs on the protoboard.
- 9. Close the NI ELVIS II Instrument Launcher strip.

End of Exercise 5.3

Exercise 5.4: LabVIEW Logic State Analyzer

The previous exercises have covered only the state of digital outputs at one point in time. This exercise shows how you can form a timing diagram by stringing sequential states together sampled uniformly in time. Plotting several digital lines together on the same graph generates a digital timing diagram as illustrated in Figure 5.7.

A binary counter has a unique timing diagram where the falling edge of the previous bit causes the next bit to toggle.



Figure 5.7. Timing Diagram of a four bit Binary Counter

Using the LabVIEW APIs for the digital I/O, you can build a simple 4-bit logic state analyzer. The Digital I/O palette is located in **Functions**»**Programming**»**Measurement I/O**»**NI ELVISmx**»**NI ELVISmx Digital Reader**.



Figure 5.8. Location of NI ELVISmx Digital Reader

Launch LabVIEW and then open **Binary CounterMx.vi** from the Hands-On-NI ELVIS II library folder.

In the Block Diagram, the NI-ELVISmx Digital Reader has been initialized to use lines 0 to 7 (blue ring constant) for input from the protoboard.

Note: In this example, the NI ELVIS USB communication port is Device 3. Depending on how many DAQ cards you have in you computer, it could be Device 1, 2, or 3. With only the NI ELVIS USB port available, it would be Device 1. Change the Dev # to match your NI ELVIS II.



Figure 5.9. Block Diagram for the program Binary CounterMx.vi

The 4-bit logic state analyzer samples NI ELVIS lines <0..7> and presents the line states as a Boolean array (thick green line). The index arrays extract bits <0..3> (Q1, Q2, Q3, Q4) to the respective trace indicators and then into a numeric value (0 or 1) for bundling with the other traces for the timing diagram plot. With the many LabVIEW chart format options, you can present the data in a timing diagram format.

A copy of the data also goes to the AND gate, where bits <4..7> are set to zero. The resultant data is converted to a numeric (0 to 15) and presented on the front panel.

End of Exercise 5.4

Multisim Challenge: Design an 8-bit Digital Counter Circuit

Design an 8-bit decimal counter with two 7-segment displays. Use a 555 timer IC to generate the clock signal.

1. Launch Multisim and open **555 Timer Binary Counter** from the NI ELVIS II program library. In this program, is simulated the same circuit elements used in *Exercise 5.3: Building a 4-bit Digital Counter*.



Figure 5.10. Multisim schmatic of the visualization of a 4-bit Binary Counter

- 2. Double-click on the scope icon XSC2. A 4-channel oscilloscope display appears.
- 3. Run this simulation by clicking on the green arrow. Observe that the 4channel display is similar to the real circuit built on an NI ELVIS II protoboard. Stop the simulation by clicking on the red square.
- 4. Open a second program called **Decimal Counter**. This program replaces the binary counter with a decimal counter (7490N), adds a 7-segment driver (7447N) IC, and adds a 7-segment display. Note that the current limiting resistors for the 7-segment LEDs are found in the resistor pack.
- 5. Run this program to see a single-digit counter with a 7-segment display.



Figure 5.11. Decimal Reading of a 4-bit Binary Counter

- 6. Stop the simulation and add a second 7490N, a 7448N, a Resistor pack 330 Ω , and a 7-segment display to the Multisim circuit. You can implement this with a simple copy and paste of the components already on the circuit diagram. Alternatively, you can find a list of components by browsing to **PlaceComponent**.
- 7. Connect the output QD of the first counter chip (7490N) to the input INA of the second counter chip (7448N). Together these chips form a two-digit counter counting from 00 to 99. This is shown in the file, **Decimal CounterX2.**
- 8. Connect the other virtual wires to the added chips to build a two-digit decimal counter.
- 9. Run the simulation.